REMARKS

Entry of this amendment is respectfully requested on the grounds that applicant is responding to a new ground of rejection, made for the first time in the Final Office action. Accordingly, applicant has not had a prior opportunity to respond to the new ground of rejection. Entry of this amendment is also requested on the grounds that it places the claims in better condition for appeal.

Alternatively, applicant requests that the finality of the March 20 Office action be withdrawn. Although the Office action summary indicates that the action is final, there is no discussion in the body of the Office action indicating that applicant's previous amendment necessitated the new ground of rejection. Thus, because the Office *sua sponte* entered a new ground of rejection, that rejection should not be made final.

In paragraph 7 of the Office action, claims 11, 13-31, and 33-58 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over published application 2002-0078316 to Nakamura (hereinafter "Nakamura"). The examiner recognizes that "Nakamura does not specifically teach the processor simultaneously accesses [accessing] more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible as well as each memory bank having separate circuitry." It is respectfully submitted that the examiner's construction of Nakamura is not reasonable. It can be seen from Figure 2 and the corresponding description in the specification of Nakamura that each of the banks has a row decoder (RDEC) and a column decoder (CDEC). However, it is further seen from Figure 2 that the address buffer 14 is common for all of the banks. Whatever address is received by the address buffer, is input to all of the banks. If the examiner is correct in her assertion that simultaneous access is "clearly implied by the figures," then the examiner must acknowledge that the only type of simultaneous access that is possible, is to simultaneously access the same address in each of the memory banks. The examiner will recognize that simultaneously accessing the same address in each of the memory banks is not particularly useful. Unless great care is taken in writing of the data, it is virtually impossible for the data needed by the microprocessor to be found in exactly the same address in each of the banks. Thus, it is respectfully submitted that the examiner reads too much into Nakamura when the examiner concludes that the architecture in Figure 2 indicates that simultaneous access is possible when such simultaneous access would be practically of no value.

However, to further the prosecution of this application, applicant has nonetheless amended all of the independent claims, claims 11, 18, 25, 31, 37, 43, 49, and 52 to make it clear that in applicant's invention the processor may simultaneously communicate with different memory addresses in two or more of the memory banks. Because in Nakamura the same address is input to all of the banks, it is impossible to communicate with different memory addresses in two or more of the banks. It is therefore

respectfully requested that the 35 U.S.C. § 103 rejection of claims 11, 18, 25, 31, 37, 43, 49, and 52, together with their dependent claims, be withdrawn.

Applicant has made a diligent effort to place the claims in condition for allowance. Accordingly, a Notice of Allowance for claims 11, 13 - 31, and 33 - 58 is respectfully requested. If the examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the examiner is respectfully requested to contact applicant's attorney at the telephone number listed below so that additional changes may be discussed.

Respectfully submitted,

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